REMARKS

The claims are claims 1, 3, 5 to 9, 10, 13, 14 and 17 to 19.

Claims 1, 3, 5, 6, 10 and 13 have been amended. Claims 2, 4, 9, 11, 12, 15 and 16 are canceled. Claim 1 is amended to clarify subject matter and distinguish over the reference. Claim 3 has been amended to include the limitations of canceled claim 4. Claims 5 and 6 have both been amended into independent form incorporating the limitations of their base claim 1. Claim 10 has been amended to incorporate the limitations of canceled claims 11, 12, 15 and 16. Claim 13 is amended to depend upon amended claim 10 rather than canceled claim 11.

Claims 1 and 3 (now including subject matter originally recited in claim 4) were rejected under 35 U.S.C. 102(b) as anticipated by Kawai et al. The OFFICE ACTION states that Kawai et al discloses a digital signal processing system including a direct memory access controller 103 where each of DMA controller is coupled to each of said memory bus multiplexers and configured to access each of said memory devices via the corresponding subsystem memory bus. Regarding the subject matter of claim 4, the OFFICE ACTION states that Kawai et al discloses that each host port interface (401 and 402) is coupled to each of the memory bus multiplexers (152) and configured to access each of the memory devices via the corresponding subsystem memory bus.

Claim 1 recites subject matter not anticipated by Kawai et al. Claim 1 recites "each of the DMA controllers is coupled to each of said memory bus multiplexers of each of said plurality of processor subsystems and is configured to access each of said memory devices of each of said plurality of processor subsystems via the corresponding subsystem memory bus." This is illustrated in Figure 1 of the application where DMA controller 18 is coupled to M-bus multiplexer 16 and M-bus multiplexer 26, and where DMA controller

28 is also coupled to M-bus multiplexer 16 and M-bus multiplexer 26. Kawai et al fails to disclose this limitation that each DMA controller is coupled to each memory bus multiplexer. Figure 6 of Kawai et al shows DMA control device 103 coupled to input/output interface circuit 108 of the same digital data processor 200 which is coupled to data bus 171 and address bus 172. Figure 5 of Kawai et al shows data bus 171 and address bus 172 coupled to external data memory 201. Thus Kawai et al teaches connection of the DMA control device 103 to one address multiplexer (input/output interface circuit 108) for accessing a single memory (external data memory 201). In contrast, the recitations of claim 1 require the DMA controller to be connected to the memory multiplexers of each processor subsystem for accessing the memory of each processor subsystem. This is the equivalent of connecting the DMA control device 103 of Kawai et al to a multiplexer connected to each internal data memory 100 of each digital data processor 200. Kawai et al teaches no such connection. Accordingly, claim 1 is not anticipated by Kawai et al.

Claim 3 recites subject matter not anticipated by Kawai et al. Claim 3 recites "each of the HPI units is coupled to each of the memory bus multiplexers of each of said plurality of processor subsystems and is configured to access each of the memory devices of each of said plurality of processor subsystems via the corresponding subsystem memory bus." This is illustrated in Figure 1 where host port interface 19 is coupled to M-bus multiplexer 16 and M-bus multiplexer 26, and where host port interface 29 is also coupled to M-bus multiplexer 16 and M-bus multiplexer 26. Kawai et al fails to disclose this limitation that each host port interface is coupled to each memory bus multiplexer. Kawai et al teaches at column 14, lines 36 to 43 that I/O ports 401 and 402 illustrated in Figure 13 are connected to DMA control device 103 within the digital data processor 200. Thus the structure of Figure 13 is not

a new structure as the recited host port interface, but a substitute for the input/output interface circuit 108 illustrated in Figure 6. The OFFICE ACTION stated this structure anticipated the claimed memory bus multiplexer. Thus this cannot be a host port interface. Kawai et al likewise fails to teach that his host port interface is connected to the memory bus multiplexer of each processor subsystem for accessing the internal memory of each processor subsystem. Accordingly, claim 3 is not anticipated by Kawai et al.

The OFFICE ACTION stated at lines 1 to 3 of page 6 that claims 5 to 8 and 16 would be allowable if rewritten in independent form incorporating all the limitations of its base claim and any intervening claims. Claims 5 and 6 have each been amended to include all limitations of their base claim 1. Claims 5 and 6 are thus allowable. Claim 10 has been amended to include all limitations of claims 11, 12, 15 and 16. This subject matter corresponds to that originally recited in claim 16. Accordingly, amended claim 10 is also allowable.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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